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IEEE XPLORE GUIDE

Results for "(((delay*, defer*, deter*, wait, postpone*) <near/15> branch* <near/15> (clock*, cycle*..."

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Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

- ☐ 1. **Compaction with general synchronous timing**
 Allan, V.H.; Mueller, R.A.;
Software Engineering, IEEE Transactions on
 Volume 14, Issue 5, May 1988 Page(s):595 - 599
 Digital Object Identifier 10.1109/32.6137
[AbstractPlus](#) | Full Text: [PDF\(452 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **Incorporating interconnect, register, and clock distribution delays into the retiming process**
 Soyata, T.; Friedman, E.G.; Mulligan, J.H., Jr.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
 Volume 16, Issue 1, Jan. 1997 Page(s):105 - 120
 Digital Object Identifier 10.1109/43.559335
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(508 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **A 2.5-GFLOPS, 6.5 million polygons per second, four-way VLIW geometry processor with SII a software bypass mechanism**
 Kubosawa, H.; Higaki, N.; Ando, S.; Takahashi, H.; Asada, Y.; Anbutsu, H.; Sato, T.; Sakate, M.; S Miyake, H.; Okano, H.; Asato, A.; Kimura, Y.; Nakayama, H.; Kimoto, M.; Hirochi, K.; Saito, H.; Kai Shimada, T.;
Solid-State Circuits, IEEE Journal of
 Volume 34, Issue 11, Nov. 1999 Page(s):1619 - 1626
 Digital Object Identifier 10.1109/4.799871
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1000 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **A fully programmable sampled-data analog CMOS filter with transfer-function coefficients d**
 Vallancourt, D.; Tsvividis, Y.P.;
Solid-State Circuits, IEEE Journal of
 Volume 22, Issue 6, Dec 1987 Page(s):1022 - 1030
[AbstractPlus](#) | Full Text: [PDF\(1528 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 5. **Design methodology for synthesizing clock distribution networks exploiting nonzero localiz**
 Neves, J.L.; Friedman, E.G.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
 Volume 4, Issue 2, June 1996 Page(s):286 - 291

DB=PGPB,USPT; PLUR=YES; OP=OR

<u>L15</u>	L14 and (thread\$4 or multi near2 thread\$3)	0	<u>L15</u>
<u>L14</u>	L13 and unconditional	1	<u>L14</u>
<u>L13</u>	L12 and (compil\$5 or assembl\$5)	1	<u>L13</u>
<u>L12</u>	L7 and pipelin\$6	1	<u>L12</u>
<u>L11</u>	L9 and l4	5	<u>L11</u>
<u>L10</u>	L9 and l1	8	<u>L10</u>
<u>L9</u>	(713/401,601) [CCLS]	976	<u>L9</u>

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

<u>L8</u>	(COUNT\$3 OR NUMBER) NEAR5 (instruction\$1 OR MICROINSTRUCTION\$1) near15 (convert\$5 or translat\$6 or conversion\$1 or calculat\$4) near15 (delay\$5 or wait\$5)	53	<u>L8</u>
<u>L7</u>	5517628.pn.	2	<u>L7</u>
<u>L6</u>	L5 not l3	32	<u>L6</u>
<u>L5</u>	(detect\$5 or determin\$6 or check\$4 count\$5) near6 NUMBER NEAR5 (instruction\$1) near15 (cycle\$1 or clock\$1) near15 (delay\$5 or wait\$5)	66	<u>L5</u>
<u>L4</u>	NUMBER NEAR5 (instruction\$1) near15 (cycle\$1 or clock\$1) near15 (delay\$5 or wait\$5)	443	<u>L4</u>
<u>L3</u>	NUMBER NEAR5 (instruction\$1) near15 (cycle\$1 or clock\$1) near15 (delay\$5 or wait\$5) near15 count\$3	49	<u>L3</u>
<u>L2</u>	(instruction\$1) near15 (cycle\$1 or clock\$1) near15 (delay\$5 or wait\$5) near12 number near15 count\$3	80	<u>L2</u>
<u>L1</u>	(instruction\$1) near15 (cycle\$1 or clock\$1) near15 (delay\$5 or wait\$5) near12 number	616	<u>L1</u>

END OF SEARCH HISTORY

Digital Object Identifier 10.1109/92.502201

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(724 KB\)](#) IEEE JNL
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6. **On the complexity of designing optimal branch-and-combine clock networks**

El-Amawy, A.; Kulasinghe, P.;

[Computers, IEEE Transactions on](#)

Volume 47, Issue 2, Feb. 1998 Page(s):264 - 269

Digital Object Identifier 10.1109/12.664212

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(188 KB\)](#) IEEE JNL
[Rights and Permissions](#)

7. **A novel image rejection architecture for quadrature radio receivers**

Valkama, M.; Renfors, M.;

[Circuits and Systems II: Express Briefs, IEEE Transactions on \[see also Circuits and Systems II: A Signal Processing, IEEE Transactions on\]](#)

Volume 51, Issue 2, Feb 2004 Page(s):61 - 68

Digital Object Identifier 10.1109/TCSII.2003.822423

[AbstractPlus](#) | Full Text: [PDF\(312 KB\)](#) IEEE JNL
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8. **Retiming edge-triggered circuits under general delay models**

Lalgudi, K.N.; Papaefthymiou, M.C.;

[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)

Volume 16, Issue 12, Dec. 1997 Page(s):1393 - 1408

Digital Object Identifier 10.1109/43.664222

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